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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/705,134	11/02/2000	Alan E. Reamon	PD-99W231	6154

7590 08/07/2003

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EXAMINER	
LEE, BENNY T	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 08/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES DEPARTMENT OF COMMERCE
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09/705,134

SERIAL NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.

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	15

DATE MAILED:

This is a communication from the examiner in charge of your application.

COMMISSIONER OF PATENTS AND TRADEMARKS

☐ This application has been examined ☒ Responsive to communication filed on 12 Jun 2003 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire three (3) month(s), ____ days from the date of this letter.
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Notice re Patent Drawing, PTO-948.
3. ☐ Notice of Art Cited by Applicant, PTO-1449
4. ☐ Notice of Informal Patent Application, Form PTO-152
5. ☐ Information on How to Effect Drawing Changes, PTO-1474
6. ☐ _____

Part II SUMMARY OF ACTION

1. ☒ Claims 1, 7, 11, 12 are pending in the application.

   Of the above, claims _____ are withdrawn from consideration.

2. ☐ Claims _____ have been cancelled.

3. ☐ Claims _____ are allowed.

4. ☒ Claims 1, 7, 11 are rejected.

5. ☒ Claims 12 IS ~~are~~ objected to.

6. ☐ Claims _____ are subject to restriction or election requirement.

7. ☐ This application has been filed with informal drawings which are acceptable for examination purposes until such time as allowable subject matter is indicated.

8. ☐ Allowable subject matter having been indicated, formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on _____. These drawings are ☐ acceptable; ☐ not acceptable (see explanation).

10. ☐ The ☐ proposed drawing correction and/or the ☐ proposed additional or substitute sheet(s) of drawings, filed on _____ has (have) been ☐ approved by the examiner. ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed _____, has been ☐ approved. ☐ disapproved (see explanation). However, the Patent and Trademark Office no longer makes drawing changes. It is now applicant's responsibility to ensure that the drawings are corrected. Corrections MUST be effected in accordance with the instructions set forth on the attached letter "INFORMATION ON HOW T EFFECT DRAWING CHANGES", PTO-1474.

12. ☐ Acknowledgment is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. _____; filed on _____.

13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

PTOL-326 (Rev. 7-82) EXAMINER'S ACTION

SN 705134

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 24 April 2003 has been entered.

The disclosure is objected to because of the following informalities: Note that reference labels (2, 3, 4) need to be described with respect to fig. 1 as amended. Likewise reference labels (16^{IV}, 16^{V}, 16^{VI}) need description relative to fig. 5. Appropriate correction is required.

The drawings are objected to because of the following: In fig. 6, reference label -- 10 -- still needs to be added as per page 7, line 8 of the specification. Correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 7 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Landis (of record).

Landis (fig. 11) discloses an integrated circuit chip having an on-chip multi-layer shielded monolithic transmission line comprising top most and bottom ground layers and three part signal layer. Note that intervening layers of dielectric (e.g. 78 in Fig. 6) separate the conductive layers. Note that the center signal conducting strip is laterally spaced from terminal strips (in the same

plane) by dielectric spacer material (e.g. 78). Moreover, note that additional conductive strips electrically connect in register between terminal strips and ground planes to provide an enclosed multi-layered shielding structure surrounding signal strip. Note that of particular interest in the Fig. 11 embodiment is that the distance between the top & bottom ground layers is the same as the distance between the terminal strips, by virtue of the simulated "circular" configuration which provides for a same diameter relative to the center of the configuration.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Landis (of record).

Note that fig. 10 discloses an integrated circuit chip having on-chip multi-layer shielded monolithic transmission line arrangement comprising a plurality of laterally spaced signal strips (96) which are individually surrounded and shielded by ground planes (70, 92) and side walls (94). Moreover, note that the plural arrangement of fig. 10 is manufactured in the like manner for the signal transmission line arrangement (e.g. see fig. 8). However, the fig. 10 embodiment does not disclose that the plural transmission line arrangement has a spacing between upper and lower ground layers which is the same as a spacing between lateral spaced strips.

As described above in the preceding rejection, the Fig. 11 embodiment discloses an on-chip transmission line arrangement where the spacing of the upper and lower ground layers is the same as the spacing between laterally spaced strips by virtue of it's quasi circular configuration thus resulting in a substantially same diameter throughout the transmission line arrangement.

Accordingly, it would have been obvious to have realized the rectangular shaped shielded transmission line arrangements in the Fig. 10 embodiments as transmission line arrangements having the configuration of Fig. 11. Such a modification would have been considered an obvious substitution of art recognized equivalent transmission line arrangements, especially since the fig. 11 embodiment would have function in the same manner as the transmission line arrangements in Fig. 10, thereby suggesting the obviousness of such a modification.

Applicant's arguments filed 24 April 2003 have been fully considered but they are not persuasive.

Applicants' have argued that the Landis reference fails to "remotely show or suggest an integrated circuit chip having an on-chip monolithic transmission line". Moreover, applicants' emphasizes that there is a fundamental difference between the "circuit board" (as disclosed by Landis) which "simply comprises various conductive structures" as compared to "an integrated circuit" (as claimed by applicants') which "is comprised of various circuit elements".

With respect to applicants' argument, it should be noted that Landis indeed is an considered an "integrated circuit" having "on-chip" arrangement. As is evident from, for example, figs. 1 & 3, the shielded transmission line arrangements are "embedded" in a substrate which is suitable for "IC" (i.e. integrated circuit or "chip") applications and thus are indeed considered "on-chip". Moreover, it should be noted that a comparison of the structure of applicants' invention (e.g. figs. 3, 4) to the structure in Landis appears to show substantially similar configurations. In particular, the shield "on-chip" transmission line in figs. 3, 4 of applicants' invention is disposed over a substrate in much the same manner as the shielded transmission line in Landis is disposed over the substrate (69, 20) in Fig. 7 of Landis. Accordingly, given the substantially similar configurations between applicants' invention and the Landis reference, it can be reasonably assumed that the Landis "circuit board" can be considered an "integrated circuit chip" much in the same manner that applicants' inventive configuration can be considered an "integrated circuit chip". While applicants' argue that an "integrated circuit chip" comprises "circuit elements", it should be noted that applicants' inventive "integrated circuit chip" appears only to disclose the shielded transmission line without any disclosure of "circuit elements" needed

to define an "integrated circuit chip". Accordingly, if applicants' invention of a shielded transmission line over a substrate (e.g. Figs. 3, 4) can be defined as an "integrated circuit chip", then it stands to reason than any like structure (i.e. Landis) can likewise be considered an "integrated circuit chip". In other words, the lack of any claimed "circuit elements" recited in the body of the claims being associated with the preamble recitation of the "integrated circuit chip" would thus provide no patentable weight to such a preamble limitation.

With respect to the rejection of claim 11 as being obvious in view of Landis, applicants' also argue that there is no suggestion of an integrated circuit chip with an on-chip transmission line. Accordingly, the above rebuttal of applicants' argument similarly applies to the rejection of claim 11.

Accordingly, for reasons set forth in the above rejections and rebuttal of applicants' arguments, the rejections continue to stand.

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benny Lee whose telephone number is (703) 308 4902.

BENNY T. LEE
PRIMARY EXAMINER
ART UNIT 2817

B. Lee

August 6, 2003